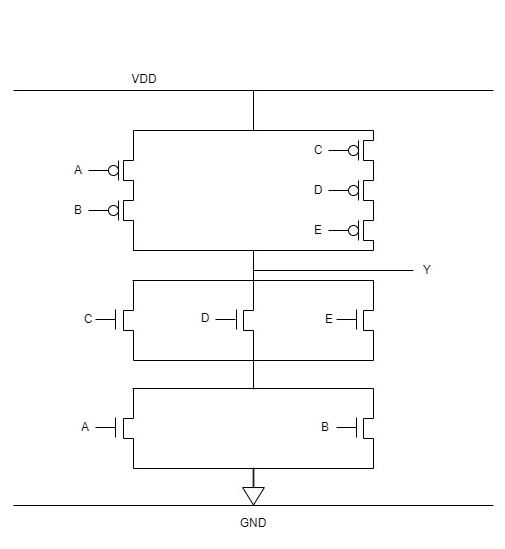
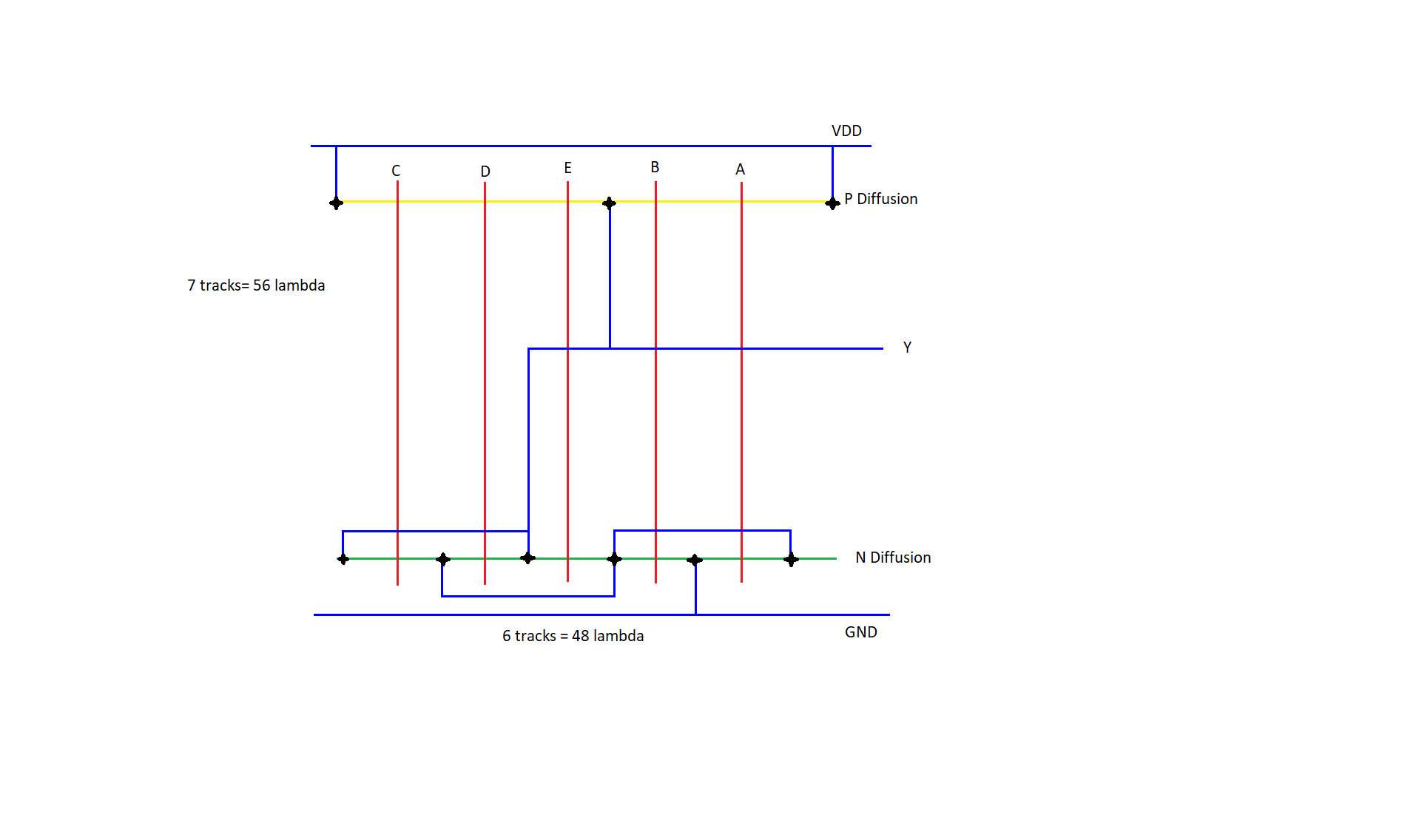
**Assignment-1**

Given 5 input function:

**Transistor level CMOS logic diagram:**

**Stick Diagram with area estimation:**



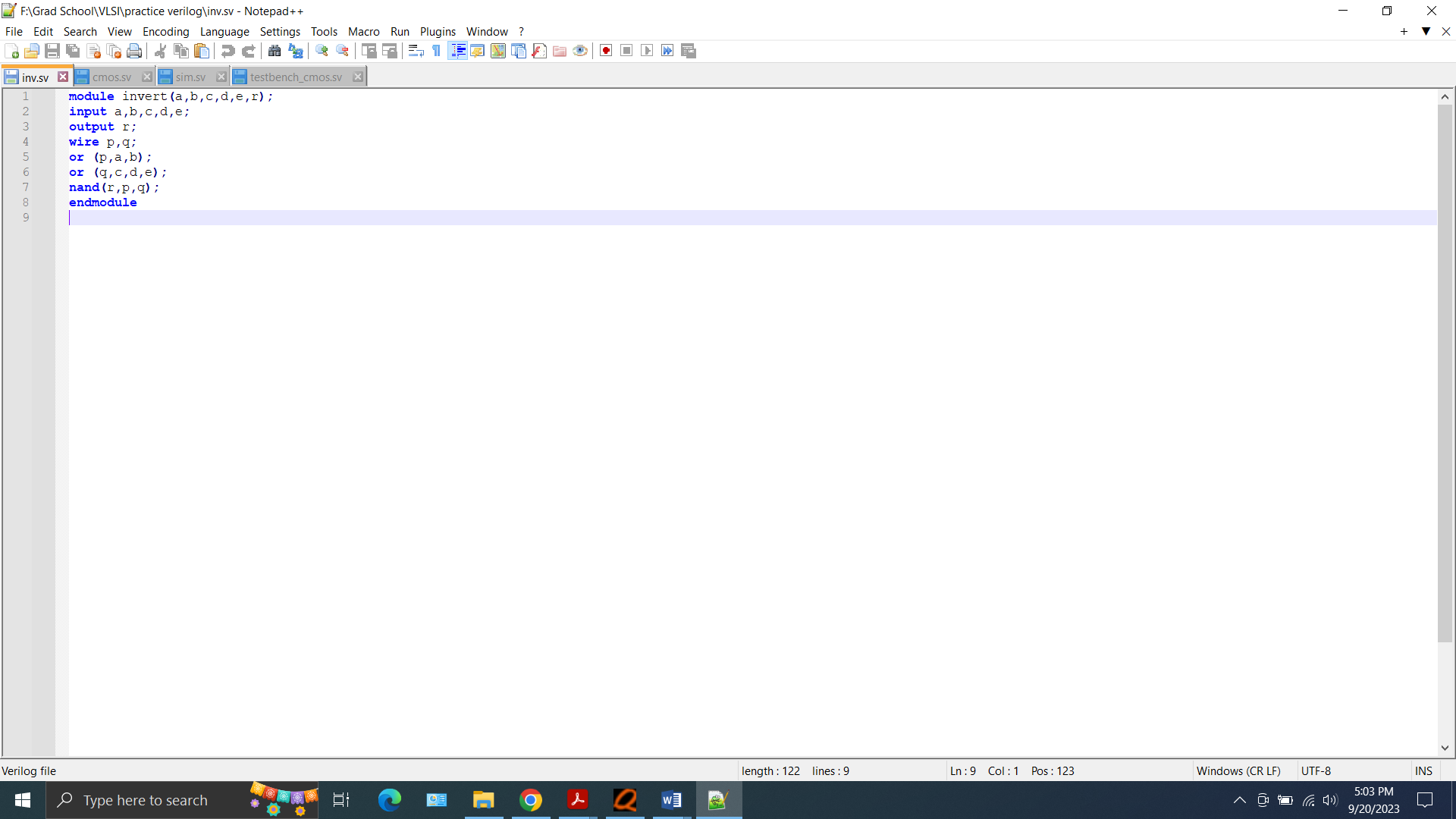
Total estimated area:

Vertically 7 tracks = 7 X 8 λ =56 λ

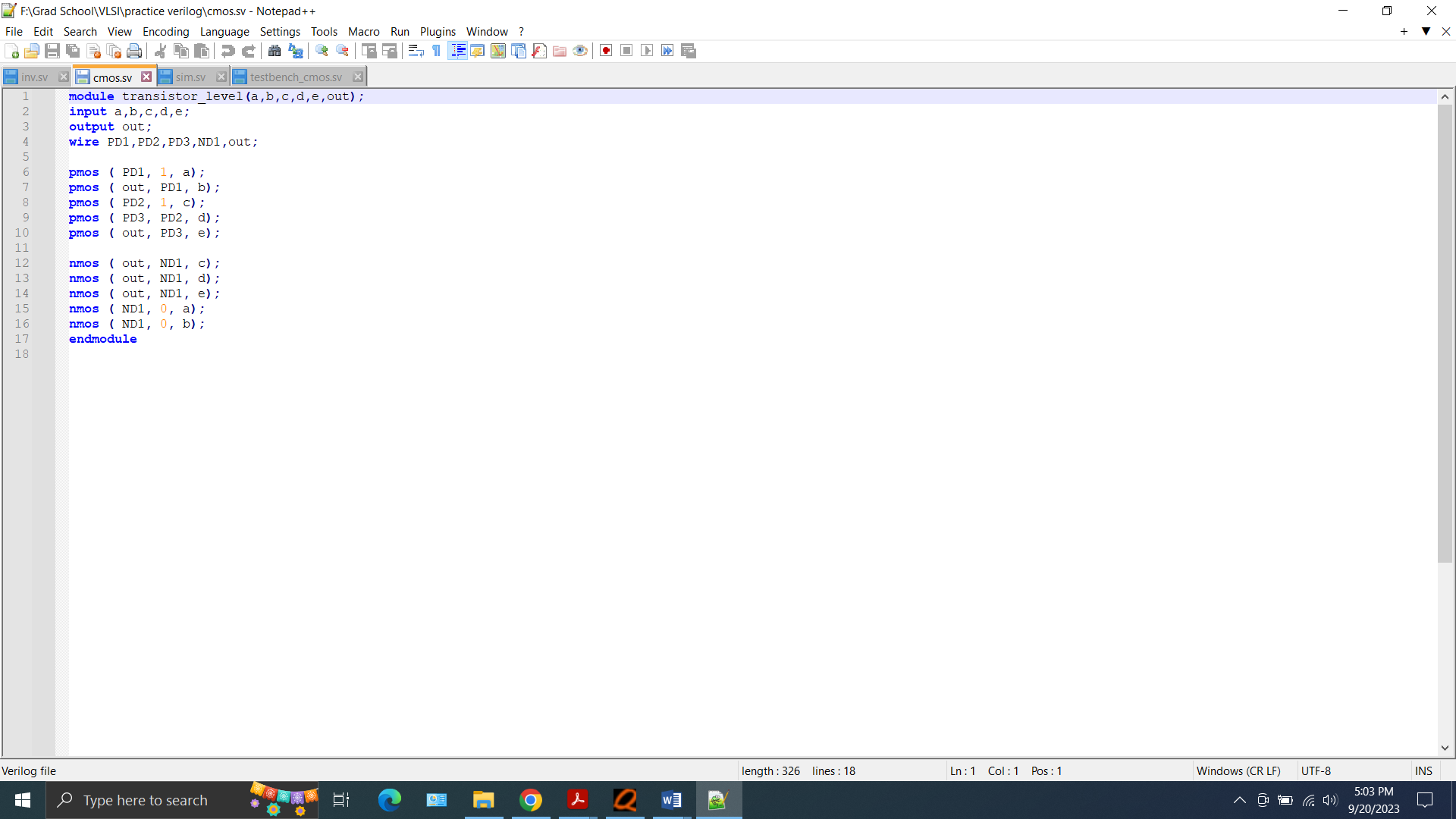
Horizontally 7 tracks = 6 X 8 λ =48 λ

Total area =56 λ X 48 λ

Gate level module:

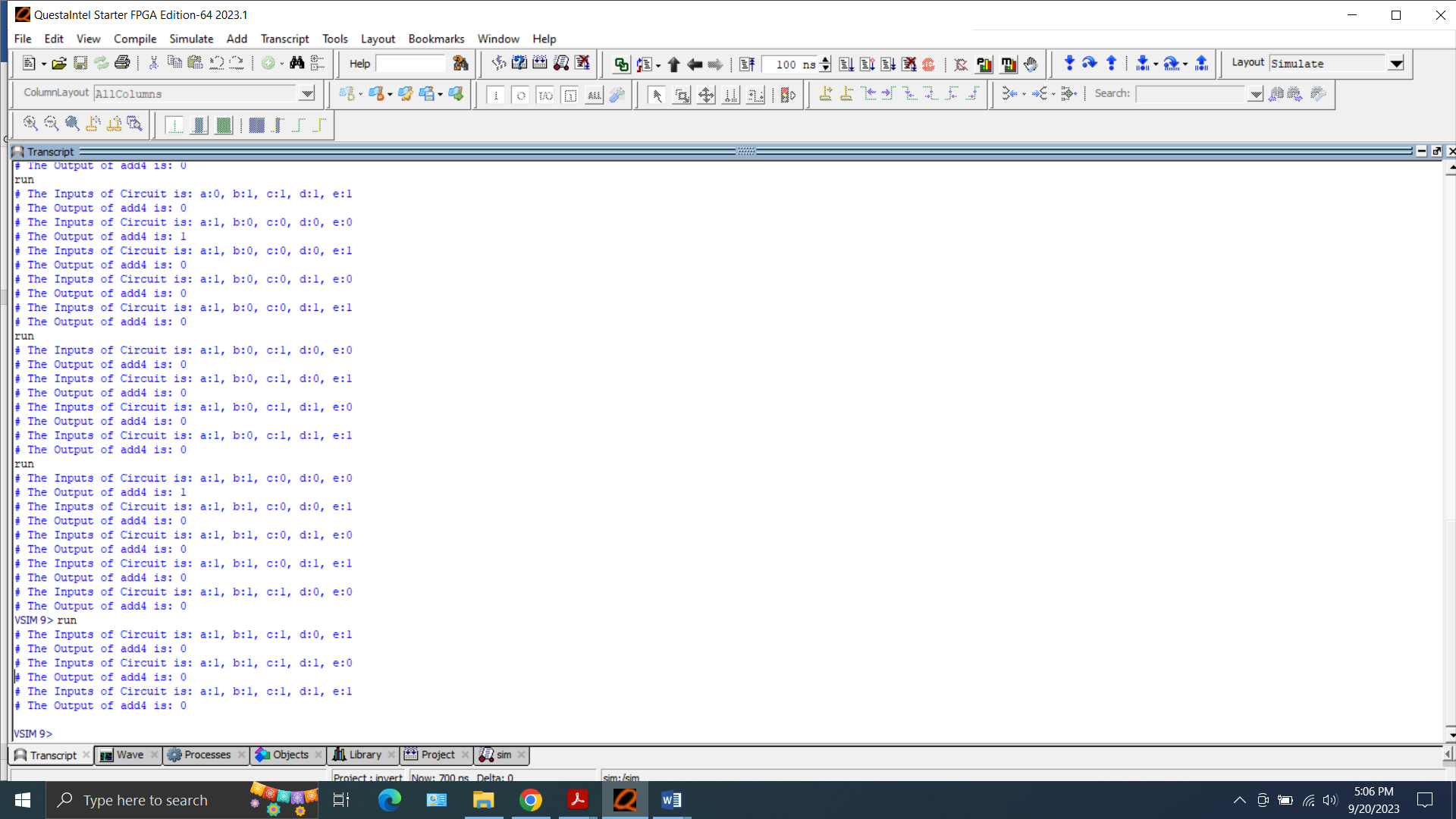
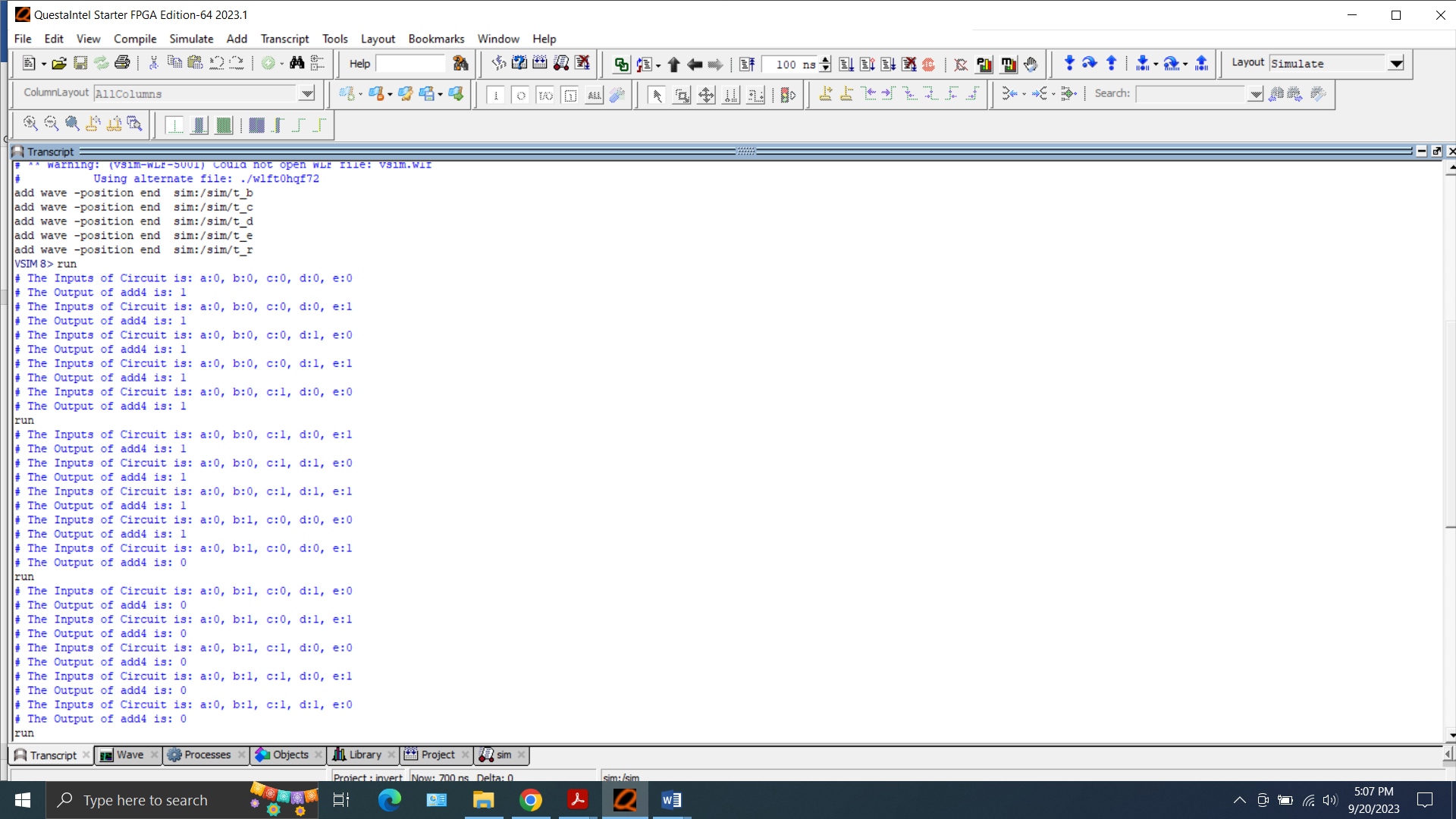


Transistor level module:

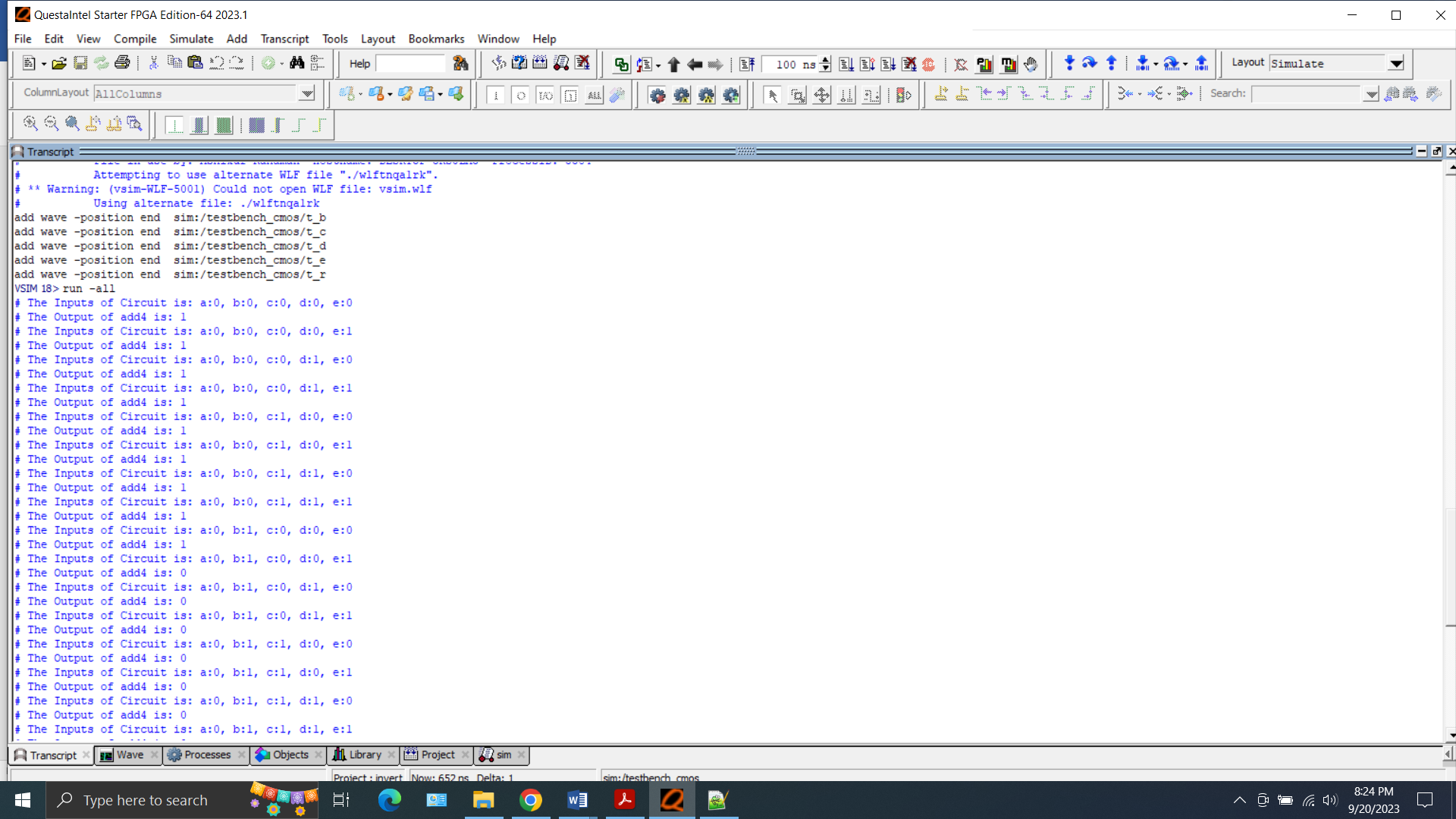


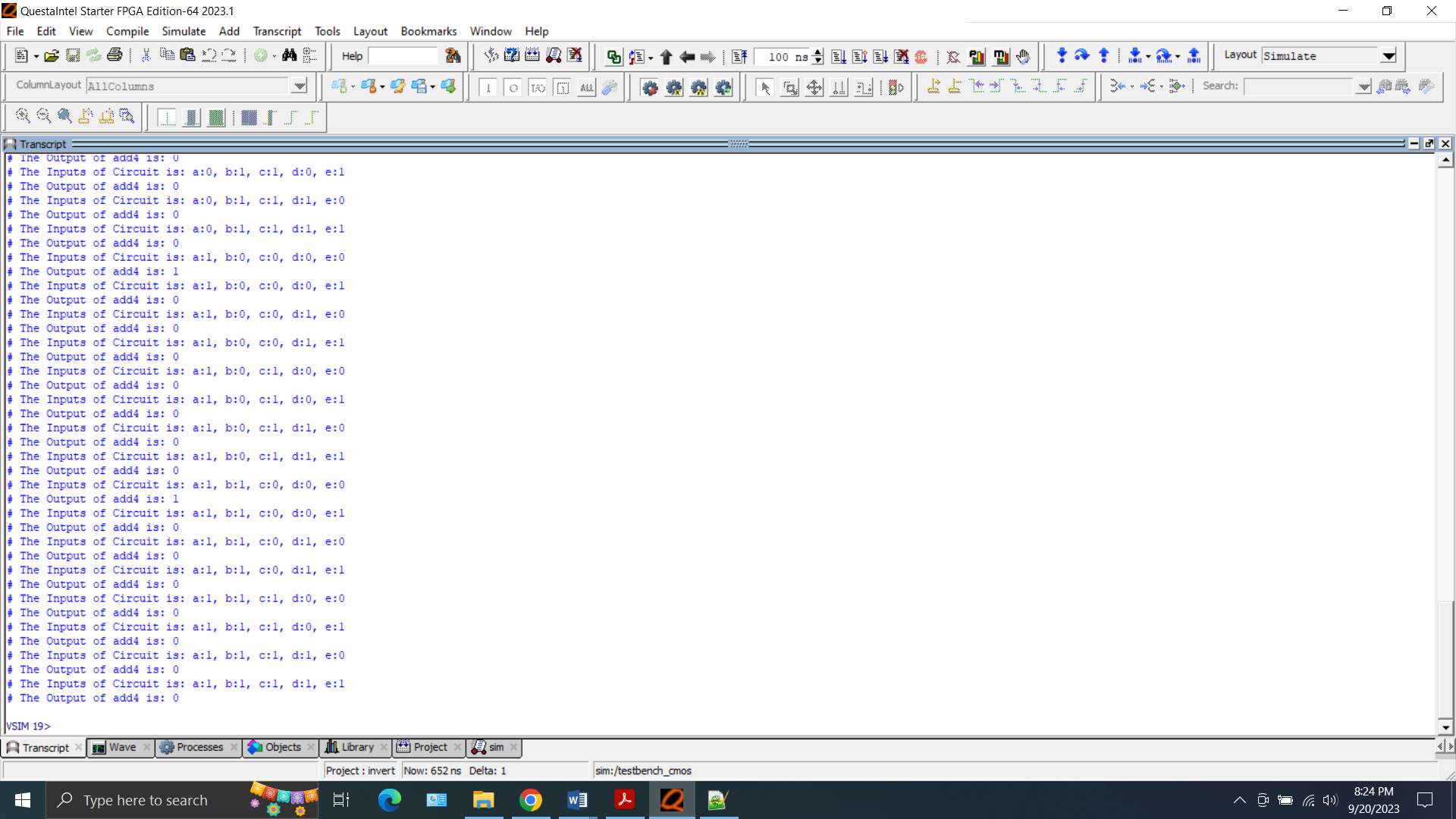
Questa output for all 32 possible combinations (for gate level and transistor level the outputs are same)

Gate level:

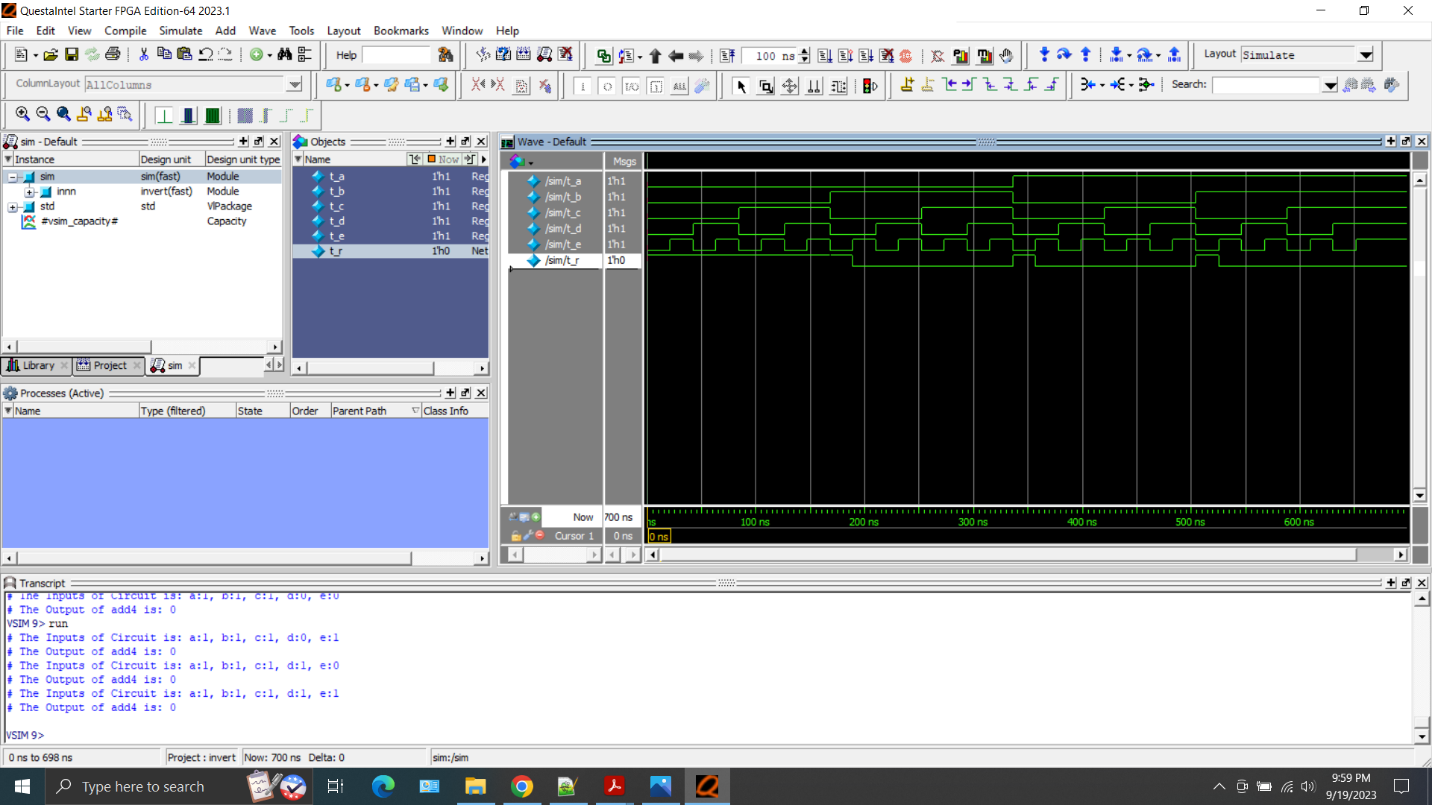


Transistor level:





Wave form of gate level:



Wave form of transistor level:

